Advanced Hardware Neural Network Architectures Using Embedded Multi-Core Processors

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Keywords: spiking neural networks, hardware implementation, benchmark dataset classification

Spiking neurons (SNs) [1] differ from conventional artificial neural network (ANN) models as information is transmitted by means of spikes rather than by firing rates. It is believed that this allows SNs to have richer dynamics as they can exploit the temporal domain to encode or decode data in the form of spike trains. However, this has demanded the development of new learning rules drawing again on inspiration from biology. When implemented on parallel hardware, neural networks (NNs) can take full advantage of their inherent parallelism allowing for specific units to be designed and added that boost the computing speed. Hence, these circuits will run orders of magnitude faster than software simulations, becoming appropriate for real-time applications while staying low-cost.

This paper aims to report on the issues arising from the authors' experience [2] in implementing spiking neural networks on Field Programmable Gate Arrays (FPGAs). A number of challenges are identified [3] [4] that arise when facing the area in terms of creating large-scale implementations of spiking neural networks (SNNs) on Xilinx FPGAs, particularly that operate in real time, and yet demonstrate biological plausibility. The presented implementations of a SNNs, partly sacrifice the fully parallel nature of the design, by embedding soft-core microcontroller modules (Xilinx PicoBlaze or MicroBlaze). These microcontrollers do not use dedicated hardware resources of the FPGA platform. The input values of the implemented SNNs have been encoded by overlapped and graded sensitivity profiles, algorithm executed by one of the embedded cores. This multiple encoding assures that clusters will be classified flexibly. Extending the network to multiple layers it can be demonstrated, that the sequential nature of pulsing neurons can be exploited to validate the correct classification of overlapping clusters. The execution of the neuron body algorithm for all cells in the network is implemented on individual cores. Therefore, these run in parallel but still execute instructions sequentially. On the other hand, the synapse modules, where the spikes are weighted and the learning rules reside, are all built of dedicated hardware elements, yielding a pure parallel execution.

In order to test the performance and potential applicability of these advanced neural systems, benchmark tests have been implemented, using selected datasets (WINE, Echocardiogram) to build a real-time classification tool. Implementation details and measurement results are given with comparisons to other significant method's scores from the specific literature.

References

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