Implementing reconfigurable operating system components in Nios II with custom instructions

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Abstract

In this paper we introduce a possible way of hybrid computer implementation. The purpose of this topic is to realize a hardware, on which we can run, measure and benchmark the improved system responses. The main principle is the hardware development or/and replacement of operating system's critical and time-consuming processes. Our SoC hardware is developed on Cyclone II FPGA which consists of 50 MHz NIOS II soft-processor with peripheral system and basic I/O interfaces (PS/2 keyboard, JTAG console and VGA module). We utilized the NIOS II research possibility which means any custom hardware can be implemented in ALU block and can be called as additional custom instruction.

We present our key focus issues, which are the improvement of interrupt service routine, matching of a previous custom designed hardware semaphore of operating system and assigning hardware priority to software processes of operating system. Beyond the setting of custom PIO cores to NIOS II we introduce our future experiments ie. testing the built-in design by running MicroC/OS-II real time operating system on the hardware. This allows us to manage and measure the benchmark parameters on our custom non-Neumann hybrid computer.

Keywords: FPGA, reconfigurable computing, NIOS, SoPC, SoC, real-time operating system

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