Line-rate Packet Processing in Hardware: the Evolution Towards 400 Gbit/s*

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Abstract

Network packet parsing and packet forwarding is a general task for all modern network devices. However, the requirement for line-rate packet processing, independently from the transmission technology, is a common demand against core network equipments. In this paper, we investigate programmable hardware architectures (i.e., Field Programmable Gate Array - FPGA) as a central building block of the forwarding plane for state-of-the-art 100 Gbit/s network devices. We reveal the benefits and drawbacks of the available hardware architectures (such as Network Processors, Application-Specific Integrated Circuits (ASIC) and FPGAs, respectively). After showing the general packet processing steps on programmable hardware, we describe the problem space of line-rate packet processing in relation to the evolution of the transmission technologies, i.e., 1, 10, 100 Gbit/s Ethernet and beyond. Moreover, we present design trade-offs, such as operational frequency, data path width and resource requirement, covering the 1 to 400 Gbit/s throughput range and we propose best practices for their hardware designs.

Keywords: Packet Processing, Forwarding Plane, FPGA, 100 Gbit/s Ethernet

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