Implementing SoCs with reconfigurable technology

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Abstract

SoC technology became the one of the most popular choices of implementing a computing system. In addition to small size, SoCs are cheaper, more power efficient and reliable than multichip systems with the same computational power. One of their disadvantages is that a SoC still needs some additional circuitry if being used in a system that requires more than it's capabilities. One solution to this problem lies in reconfigurable technology, which had already a tendency of integrating often used functionalities in addition to reconfigurable circuitry.

CAD tools were made to assist the development of SoC systems with reconfigurable technologies. Key concepts behind these tools are IP cores and bus architectures. By providing a convenient way to pack the IP cores together, these tools speed up implementation and verification time, also enabling the creation of systems that use both traditional and special hardware components. On top of that the support of software development tools for the specific IP library is usually integrated. In this paper we overview some of the methodologies assisting implementation of SoCs within FPGAs. An example of a system built with Altera SoPC builder targeting the Altera DE2 board is also presented.

Keywords: SoC, reconfigurable hardware, FPGA

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